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Patentanmeldung Nr. Patent application No. Demande de brevet n°

02102849.3

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R C van Dijk



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DESCRIPTION

## POWER SUPPLY LEVEL MONITORING AND RESET GENERATION

## Field of the invention

- 5 The present invention concerns systems where the power supply level is being monitored by means of a dedicated monitor. More particularly, this invention relates to integrated circuits comprising a power supply level monitor.

## Background of the invention

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Integrated circuits require a supply voltage for operation. In order for an integrated circuit to operate reliably, the supply voltage has to be stable. After power-on or after a reset, the supply voltage typically requires some time to reach a stable level.

- 15 It is state of the art to employ a special circuitry, sometimes called power on reset (POR) circuitry, in an integrated circuit that compares the power supply level with the level of an internal reference voltage. In order for such a special circuitry to function properly, the internal reference has to start more quickly than the supply voltage. This state of the art approach is not very robust, since the ramping up of the reference voltage may be delayed,
- 20 for example. It is another disadvantage of this known approach that the special circuitry is hard-wired. Changes are thus not possible without changing the chip layout.

- The ramping up of the supply voltage is usually not predictable, since batteries may have reached a low state or since the current load on the integrated circuitry may change. This is
- 25 another problem that can not be handled by conventional approaches.

It is thus an objective of the present invention to provide a method for reliably monitoring the level of a supply voltage, to provide a monitor for reliably monitoring the level of a supply voltage, and to provide integrated circuits based thereon.

30

## SUMMARY OF THE INVENTION

An apparatus in accordance with the present invention is claimed in claim 1.

5 Various advantageous embodiments are claimed in claims 2 through 10.

A method in accordance with the present invention is claimed in claim 11.

Various advantageous methods are claimed in claims 11, 12 and 13.

10

An integrated circuit in accordance with the present invention is claimed in claim 14.

Immediate benefits of this invention are improved reliability, flexibility, and competitiveness.

15

It is an advantage of the power supply level monitor presented herein that it can be employed as monitor and level detector in all kinds of integrated circuits.

20 The present invention avoids the problems of conventional systems using an internal reference voltage for comparison with the supply voltage.

Other advantages of the present invention are addressed in connection with the detailed embodiments.

25

### Brief description of the drawings

For a more complete description of the present invention and for further objects and advantages thereof, reference is made to the following description, taken in conjunction with  
5 the accompanying drawings, in which:

- FIG. 1A is a schematic block diagram of a first apparatus, according to the present invention;
- FIG. 1B is a schematic block diagram of the POR\_1 unit of the first apparatus;
- 10 FIG. 1C is a schematic block diagram of the POR\_2 unit of the first apparatus;
- FIG. 2A is a schematic block diagram of a second apparatus, according to the present invention;
- FIG. 2B is a schematic block diagram of the POR\_1 unit of the second apparatus;
- FIG. 2C is a schematic block diagram of the POR\_2 unit of the second apparatus;
- 15 FIG. 3 is a schematic block diagram of another POR\_1 unit, according to the present invention;
- FIG. 4 is a schematic graph used to describe the function of a POR\_1 unit, according to the present invention;
- FIG. 5 is a schematic graph used to describe the function of a POR\_2 unit, according to the present invention.
- 20

### DESCRIPTION OF PREFERRED EMBODIMENTS

The present invention is based on the following principle. An apparatus serving as monitor is  
25 provided that generates a signal (nporst) measuring the supply voltage (VDDA) and deciding whether or not this supply voltage has reached a secure level before starting a (digital) application within an integrated circuit.

The monitor according to the present invention is very flexible. In some embodiment, its  
30 delay after a reset event can be programmed.

The generation of a signal (nporst) is fundamental in many systems. The signal nporst is for example important for systems where no external reset signal can be generated. The task is to

monitor the power supply level with a stable reference voltage, which is usually identified by a bandgap voltage of a transistor. In the integrated circuit field this system can be fundamental.

5 The following problems are faced:

- can one be confident about the start-up behavior of the reference voltage (e.g, the bandgap voltage) until it is stable?
- If the bandgap rise time should be too long (or unpredictable) for a certain application, what happens in such a situation?

10

The present invention provides a solution and an architecture based thereon that is designed to overcome these uncertainties.

In Fig. 1A a schematic block diagram of a POR circuit 10, according to the present invention, is given. The POR circuit 10 generates a logic signal (nporst) indicating that a supply voltage (VDDA) has reached a stable level. This logic signal nporst is generated after a trigger signal nporst was received. The POR circuit 10 comprises a first unit 11 (POR\_1) for comparing an internal reference voltage (vref) with a voltage (Vtrl) that is a fraction of the supply voltage (VDDA) in order to issue a first logic signal (out\_res) at an output 14 as soon as the voltage (Vtrl) reaches the reference voltage (vref). A second unit 12 (POR\_2) is provided which applies a delay in order to issue a second logic signal (out\_delay) that is delayed by a delay time. A logic unit 13 is employed for combining the first logic signal (out\_res) and the second logic signal (out\_delay) in order to provide the logic signal (nporst). When this logic signal (nporst) turns logic "1", the supply voltage VDDA is deemed to be stable.

The logic unit 13 may comprise a two-port AND gate, for example.

The delay introduced by the unit POR\_2 may be programmable, as illustrated in Fig. 1A. This can be done by applying a sequence of n-bits to the programmable input 18 (Sel<n:0>). As indicated in Fig. 1A, the unit 11 may be connected to the unit 12 via an enabling line 17, that allows the unit 12 to be enabled by a signal provided by the unit 11. This enabling line 17 as well as the programmable delay are optional features.

After having described the basic principle of the present invention, details of the units POR\_1 and POR\_2 are addressed in connection with Fig. 1B and Fig. 1C, respectively.

5 The POR\_1 unit 11 comprises a voltage divider 11.1 and a comparator 11.2, as depicted in Fig. 1B. A fundamental signal that this unit 11 needs is a voltage reference like a bandgap reference. This voltage reference  $v_{ref}$  is fed to the negative input (INN) 11.4 of the comparator 11.2. The voltage divider 11.1 provides an input\_plus output signal at an output 11.3. The input\_plus voltage may be a sub-voltage of  $V_{DDA}$ , for example. The voltage divider 11.1 may be realized using resistors, MOS or CMOS devices, capacitors or  
10 other circuits. Well suited is a resistor divider comprising a tunable resistor. The voltage input\_plus is a fraction of  $V_{DDA}$ , i.e.,  $input\_plus < V_{DDA}$ . In the present embodiment, the voltage input\_plus is a fixed voltage in the range between 0V and  $V_{DDA}$ . When the voltage input\_plus at the connection line 11.3 reaches the level of the voltage reference  $v_{ref}$ , the signal out\_res at the output 14 becomes a logic "1".

15 The POR\_2 unit 12 comprises a delay unit 12.1, as depicted in Fig. 1C. Preferably, the delay time can be programmed by applying an n-bit word  $Sel_{<n:0>}$  to the select input 18. In a less complex embodiment, the delay time may be fixed. When being enabled via the enable line 17, the POR\_2 unit 12 issues a delayed signal out\_delay at the output 15.  
20 The delay unit 12.1 should be designed to provide a reasonable delay on its output (out\_delay).

In Fig. 2A, a schematic block diagram of another POR circuit 20, according to the present invention, is given. The POR circuit 20 comprises two POR units 21 and 22 (POR\_1 and  
25 POR\_2) and a logic unit 23 that is needed to combine the two digital outputs 24, 25 (out\_res and out\_delay) of POR\_1 and POR\_2. The POR circuit 20 combines the following two logic signals out\_res and out\_delay: out\_res is derived from a comparison between a bandgap voltage ( $v_{ref}$ ) and a divider voltage (input\_plus in the present embodiment); out\_delay is derived from a comparison between a divider voltage ( $v_{sel}$ ) and a  
30 delayed voltage (delay\_sig) generated by a fixed-delay block 22.1. The delayed voltage (delay\_sig) is an analog signal. The delayed voltage (delay\_sig) rises much slower than the voltage  $v_{sel}$  due to the delay introduced by the fixed-delay unit 22.1. The two logic signals

out\_res and out\_delay are combined together by the logic unit 23 which in turn generates the nporst signal at an output 26. When this logic signal nporst turns logic "1", the supply voltage VDDA is deemed to be stable. The nporst signal brings the information regarding whether or not the VDDA voltage has reached a secure level allowing the applications within  
 5 the integrated circuit to be started.

The POR\_1 unit 21 of Fig. 2B comprises logic elements that are designed in order to be able to compare a sub-voltage of VDDA (referred to as input\_plus) with a reference voltage vref. The POR\_1 unit 21 comprises a voltage divider 21.1 and a comparator 21.2. The  
 10 voltage divider 21.1 may be realized using resistors, MOS or CMOS devices, capacitors or other circuits. Well suited is a resistor divider comprising a tunable resistor. The reference voltage vref is applied to the negative input (INN) 21.4 of the comparator 21.2 of the POR\_1 unit 21. The reference voltage input\_plus is applied to the positive input (INP) of the comparator 21.2. The reference voltage input\_plus is a fraction of VDDA. Input\_plus  
 15 may be equal to vref. In the present embodiment, the POR\_1 unit 21 issues a logic "1" at the output 24 if the reference voltage input\_plus is equal to or larger than the reference voltage vref.

The POR\_2 unit 22, as depicted in Fig. 2C, comprises logic elements that are designed in  
 20 order to be able to apply a delay. It comprises a fixed-delay block 22.1 and a comparator 22.2. The delay is programmable by applying some bits Sel<n:0> to a select input 21.5 of the POR\_1 unit 21. By changing the bits applied to this input 21.5, the level of the voltage Vsel at the output 28 of the voltage divider 21.1 is adjusted. The fixed-delay block 22.1 takes the supply voltage VDDA as an input signal and delays this input signal by a fixed  
 25 delay. As a result, a delayed output signal delay\_sig is provided at the output 22.3. An example of such a delayed output signal is depicted next to the output line 22.3. The delayed signal may be a signal that rises steadily until it reaches a stable level. The delayed output signal delay\_sig is applied to the positive input (INP) of the comparator 22.2 and the voltage Vsel is applied to the negative input (INN) of the comparator 22.2. In the present  
 30 embodiment, the POR\_2 unit 22 issues a logic "1" at the output 25 after the delay, i.e., when the delayed output signal delay\_sig crosses (exceeds) the level of the voltage Vsel. Details are addressed in connection with Fig. 5 to be discussed later.

The fixed-delay unit 22.1 should be designed to provide a reasonable delay on its output (delay\_sig). The delay\_sig starts from 0 V and preferably rises up to the level of VDDA. The total delay applied to the nporst is defined by the fixed-delay unit 22.1 and the Vsel level chosen via the bit-word at the select input 21.5. Preferably, the delay time is only effective after the supply voltage VDDA was switched on or after a reset event.

Only when both logic signals out\_res and out\_delay are logic "1", the supply voltage VDDA is deemed to have reached a stable state and the signal nporst at output 26 becomes a true logic "1". The signal nporst is much more reliable than the conventional signal nporst.

The POR\_1 unit 21 may have an enable output 27 being connected to an input of the POR\_2 unit 22.

Yet another POR\_1 unit 31 is depicted in Fig. 3. The POR\_1 unit 31 comprises a voltage divider 31.1, a switch 31.6, and a comparator 31.2, as depicted in Fig. 3. A fundamental signal that this unit 31 needs is a voltage reference vref like a bandgap reference for instance. This voltage reference vref is fed to the negative input (INN) 31.4 of the comparator 31.2. The voltage divider 31.1 provides two output signals Vtrl and Vsel at the outputs 31.8 and 31.9. Both voltages Vtrl and Vsel are fractions of the VDDA voltage (also referred to as sub-voltages of VDDA). The signal nporst is applied to an input 31.7 of the switch 31.6. The signal nporst is a signal that is fed from the output 26 to the switch 31.6, for instance. When the signal nporst is logic "1" (typically after a reset event), the switch 31.6 is switched to the state denoted by a 1 and the voltage Vtrl is connected to the positive input (INP) 31.3 of the comparator 31.2. If the signal nporst is logic "0", the switch 31.6 is switched to the state denoted by a 0 and the voltage Vsel is connected to the positive input (INP) 31.3 of the comparator 31.2. The switch 31.6 enables the circuit 31 to use two different voltage levels (trip levels) to be compared with the reference voltage vref at input 31.4. The voltage Vtrl is used after a reset event (i.e., when the signal nporst is logic "1"). In this case the voltage Vtrl is about to rise as the voltage VDDA rises, since Vtrl is a fraction of VDDA. When Vtrl reaches vref, the signal out\_res becomes logic "1". The voltage Vsel may be used in case of a power down event (i.e., when the signal nporst is logic "0"). In this case the voltage Vsel is

about to decrease as the voltage VDDA decreases, since Vsel is a fraction of VDDA. When Vsel drops below vref, the signal out\_res becomes logic "0" and circuits in the integrated circuit have to stall operations.

- 5 In an embodiment where the POR\_1 unit 31 is employed together with a POR\_2 unit, according to the present invention, the POR\_2 unit rules the switching of the nporst signal, since the delayed signal out\_delay becomes logic "1" after the signal out\_res. When the supply voltage VDDA decreases, e.g., during a power down event, the POR\_1 unit 31 rules the switching of the signal nporst.

10

According to the present invention, a method is provided for generating the logic signal nporst for usage in an integrated circuit. The logic signal nporst indicates that the supply voltage (VDDA) has reached a stable level. The method comprises the steps:

- providing a reference voltage (vref),
- 15 - comparing a sub-voltage (input\_plus) of the supply voltage (VDDA) with the reference voltage (vref) in order to provide a first logic output signal (out\_res) when the sub-voltage (input\_plus) reaches the reference voltage (vref),
- providing a second logic output signal (out\_delay) that is delayed with
- 20 respect to the supply voltage (VDDA),
- combining the first logic output signal (out\_res) and the second logic output signal (out\_delay) to switch the logic signal (nporst) from one state to another state if the first logic output signal (out\_res) and the second logic output signal (out\_delay) have the same logic value, and
- 25 - starting an application within the integrated circuit.

In a preferred embodiment of the method, the logic signal (nporst) becomes a logic "1" if the first logic output signal (out\_res) and the second logic output signal (out\_delay) both represent a logic "1". In another preferred embodiment, the delay for providing the second

30 logic output signal (out\_delay) is programmable.

As illustrated in Fig. 3, an enable signal may be applied to the comparator 31.2, via an enable line 37. The same enable signal may also be applied to the POR\_2 unit.

5 According to the present invention, the units POR\_1 and POR\_2 generate two independent logic signals out\_res and out\_delay, as described above in connection with Figs. 1A-1C, Figs. 2A-2C, and Fig. 3. Both logic signals out\_res and out\_delay may be generated using a hysteresis. The POR\_1 hysteresis is fundamental while the POR\_2 hysteresis can be avoided. The POR\_1 hysteresis should be designed to avoid possible unwanted glitches on the signal out\_res.

10 According to a preferred embodiment of the invention, the delay unit may comprise a self-biasing current generator which charges a capacitance with a current of a few nA. Such a delay unit may provide a delay of a few milliseconds. Preferably, the delay time is between 1ms and 10ms. Instead of a delay unit comprising a self-biasing current, a simple RC-delay unit  
15 may be employed.

According to the present invention, the POR circuit 10 or 20 can be designed in a manner that allows the whole circuit 10 or 20 to be disabled by applying an enable signal to the unit POR\_1, thus allowing a power-down mode. If the nporst signal generation is disabled, the  
20 nporst signal has to be fixed to the same digital level as it is when VDDA is ready and a reset is generated. This is a feature that is not necessary to make the inventive circuit 10 or 20 working, but it is an add-on feature that can be realized when a power-down mode is desired. In other words, the power-down mode is optional.

25 The supply voltage VDDA typically is a positive voltage. This voltage may be in the range between 1 Volts and 10 Volts. Preferably, the voltage VDDA is between 1.8 and 6 Volts. The nodes denoted by vss can either be connected to ground, or these nodes may be connected to a negative voltage -VDDA (double supply). The voltage VDDA may for example be +3V and the voltage vss may be -3V. The bandgap voltage vref may be 0.9V,  
30 for example. The voltage Vtrl may be 1V, for example.

Preferably, a comparator 22.2 is employed in the POR\_2 unit 22 having a comparator hysteresis of about 30mV. The comparators 11.2 and 21.2, as employed in the POR\_1 units 11 or 21 may have a comparator hysteresis of about 0V.

- 5 An integrated circuit according to the present invention may comprise a POR circuit as described in connection with Fig.1A through 3. It further comprises circuitry that requires a certain stability of the supply voltage (VDDA) before initiating operation. The integrated circuit may further comprise dedicated circuitry generating a trigger signal (nporst) after a reset event. This can be done using a conventional approach.

10

- In FIG. 4 a schematic graph is depicted. The operation of a POR\_1 unit, according to the present invention, is now described with reference to this Figure. From the schematic graph, it can be derived that initially the reference voltage  $v_{ref}$  rises more slowly than the sub-voltage  $V_{trl}$ . That is, right after a reset event, the supply voltage and thus the sub-voltage  $V_{trl}$  may rise more quickly. Between 0.9ms and 1.5ms this would lead to a logic signal  $out\_res$  being logic "1". Since the reference voltage  $v_{ref}$  exceeds the sub-voltage  $V_{trl}$  after about 1.8ms, the logic signal  $out\_res$  would suddenly become logic "0". After about 1.8ms, the logic signal  $out\_res$  becomes a logic "1" again, despite the fact that the sub-voltage  $V_{trl}$  is still not stable. Integrates circuits in a convention chip would have started operation after about 1.5ms, which is way too early in the example depicted.

- In FIG. 5 a schematic graph is depicted. The operation of a POR\_2 unit, according to the present invention, is now described with reference to this Figure. After a certain period of time (e.g., about 1.8ms), the delayed signal ( $delay\_sig$ ) starts to rise. The level of  $V_{sel}$  is adjusted (e.g., by means of programming) to a level of about 1.2V. The delayed signal ( $delay\_sig$ ) reaches the  $V_{sel}$  signal after about 8ms. Now the output signal of the POR\_2 unit becomes logic "1" and as a consequence the signal  $nporst$  turns "1". Due to the delay of about 8ms, any uncertainties as addressed in connection with Fig. 4 are ironed out. The delay can be adjusted by shifting the level of the voltage  $V_{sel}$  up or down, as indicated by the arrow 50. When shifting the level of the voltage  $V_{sel}$ , the point in time where the delayed signal ( $delay\_sig$ ) reaches  $V_{sel}$  is moved, as indicated by the arrow 51.

30

The present invention can be used in all systems that need an internal reset generation procedure. The invention is well suited for CMOS circuits.

5 It is appreciated that various features of the invention which are, for clarity, described in the context of separate embodiments may also be provided in combination in a single embodiment. Conversely, various features of the invention which are, for brevity, described in the context of a single embodiment may also be provided separately or in any suitable sub combination.

10 In the drawings and specification there has been set forth preferred embodiments of the invention and, although specific terms are used, the description thus given uses terminology in a generic and descriptive sense only and not for purposes of limitation.

CLAIMS

1. Apparatus (10; 20) for generating a logic signal (nporst) indicating that a supply voltage (VDDA) has reached a stable level, the apparatus (10; 20) comprising
  - a first unit (POR\_1, 11; 21; 31) for comparing a reference voltage (vref) with a sub-voltage (input\_plus) derived from the supply voltage (VDDA) in order to issue a first logic signal (out\_res) when the sub-voltage (input\_plus) has reached the reference voltage (vref),
  - a second unit (POR\_2, 12; 22) for applying a delay in order to issue a delayed logic signal (out\_delay),
  - a logic unit (13; 23) for combining the first logic signal (out\_res) and the delayed logic signal (out\_delay) in order to provide the logic signal (nporst).
2. The apparatus (10; 20) of claim 1, wherein the first unit (POR\_1, 11; 21; 31) comprises a voltage divider (11.1; 21.1; 31.1) and a comparator (11.2; 21.2; 31.2).
3. The apparatus (10; 20) of claim 2, wherein the first unit (POR\_1, 31) further comprises a switch (31.6) that allows a first sub-voltage (Vtrl) to be compared with the reference voltage (vref) after a reset and a second sub-voltage (Vsel) to be compared with the reference voltage (vref) after a power down.
4. The apparatus (10; 20) of claim 3, wherein a trigger signal (nporst) is applied to the switch (31.6) in order to switch it from one state to another state.
5. The apparatus (10; 20) of claim 1, 2 or 3, wherein the reference voltage (vref) is a bandgap voltage.

6. The apparatus (10; 20) of claim 1, 2 or 3, wherein the first unit (POR\_1, 21; 31) comprises an input (31.5) for programming the level of a divider voltage (Vsel), said divider voltage (Vsel) defining the delay.
- 5 7. The apparatus (10; 20) of claim 1, wherein the second unit (POR\_2, 12; 22; 32) comprises a delay unit (12.1), or a fixed delay unit (22.1) followed by a comparator (22.2).
8. The apparatus (10; 20) of claim 1, wherein the second unit (POR\_2, 12) comprises  
10 an input (18) for programming the level of a divider voltage (Vsel), said divider voltage (Vsel) defining the delay.
9. The apparatus (10; 20) of one of the preceding claims, wherein the logic unit (13; 23) comprises a two-port AND gate.
- 15 10. Method for generating a logic signal (nporst) in an integrated circuit indicating that a supply voltage (VDDA) has reached a stable level comprising the steps
  - providing a reference voltage (vref),
  - comparing a sub-voltage (input\_plus) of the supply voltage (VDDA) with  
20 the reference voltage (vref) in order to provide a first logic output signal (out\_res) when the sub-voltage (input\_plus) reaches the reference voltage (vref),
  - providing a second logic output signal (out\_delay) that is delayed with respect to the supply voltage (VDDA),
  - 25 - combining the first logic output signal (out\_res) and the second logic output signal (out\_delay) to switch the logic signal (nporst) from one state to another state if the first logic output signal (out\_res) and the second logic output signal (out\_delay) have the same logic value,
  - starting an application within the integrated circuit.

11. The method of claim 10, whereby the logic signal (nporst) becomes a logic "1" if the first logic output signal (out\_res) and the second logic output signal (out\_delay) both represent a logic "1".

5

12. The method of claim 10 or 11, comprising the step of programming the delay for providing the second logic output signal (out\_delay).

13. Integrated circuit comprising an apparatus according to one of the claims 1 through 9 and further comprising circuitry requiring a certain stability of the supply voltage (VDDA) before initiating operation.

10

15

ABSTRACT

## Power Supply Level Monitoring and RESET GENERATION

Apparatus (10) for generating a logic signal (nporst) indicating that a supply voltage (VDDA) has reached a stable level. The apparatus (10) comprises a first unit (POR\_1, 11) for  
5 comparing a reference voltage (vref) with a sub-voltage (input\_plus) derived from the supply voltage (VDDA) in order to issue a first logic signal (out\_res) when the sub-voltage (input\_plus; Vtrl, Vsel) has reached the reference voltage (vref). A second unit (POR\_2, 12; 22) is provided for applying a delay in order to issue a delayed logic signal (out\_delay). A logic unit (13) combines the first logic signal (out\_res) and the delayed logic signal  
10 (out\_delay) in order to provide the logic signal (nporst).

(Fig. 1A)

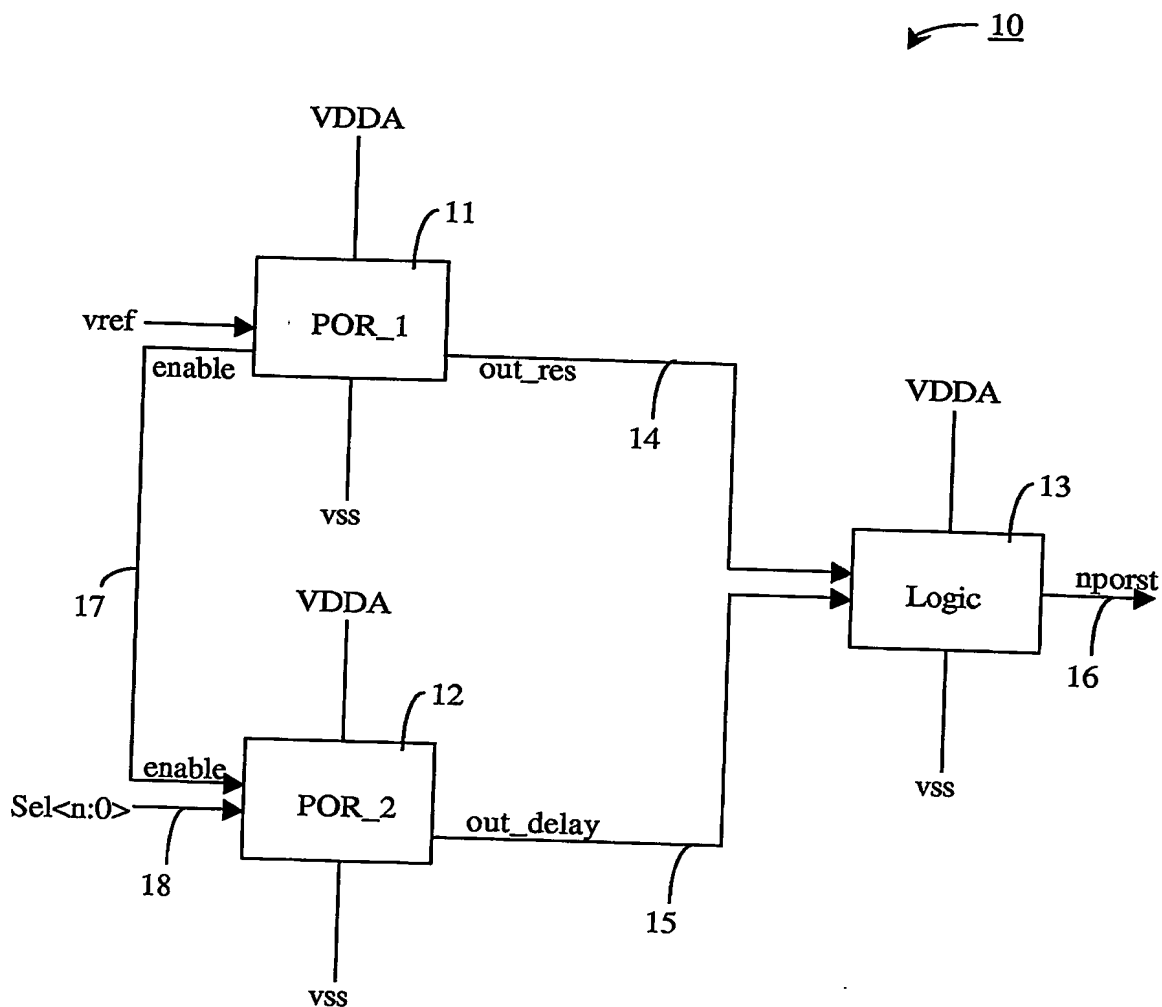


Fig. 1A

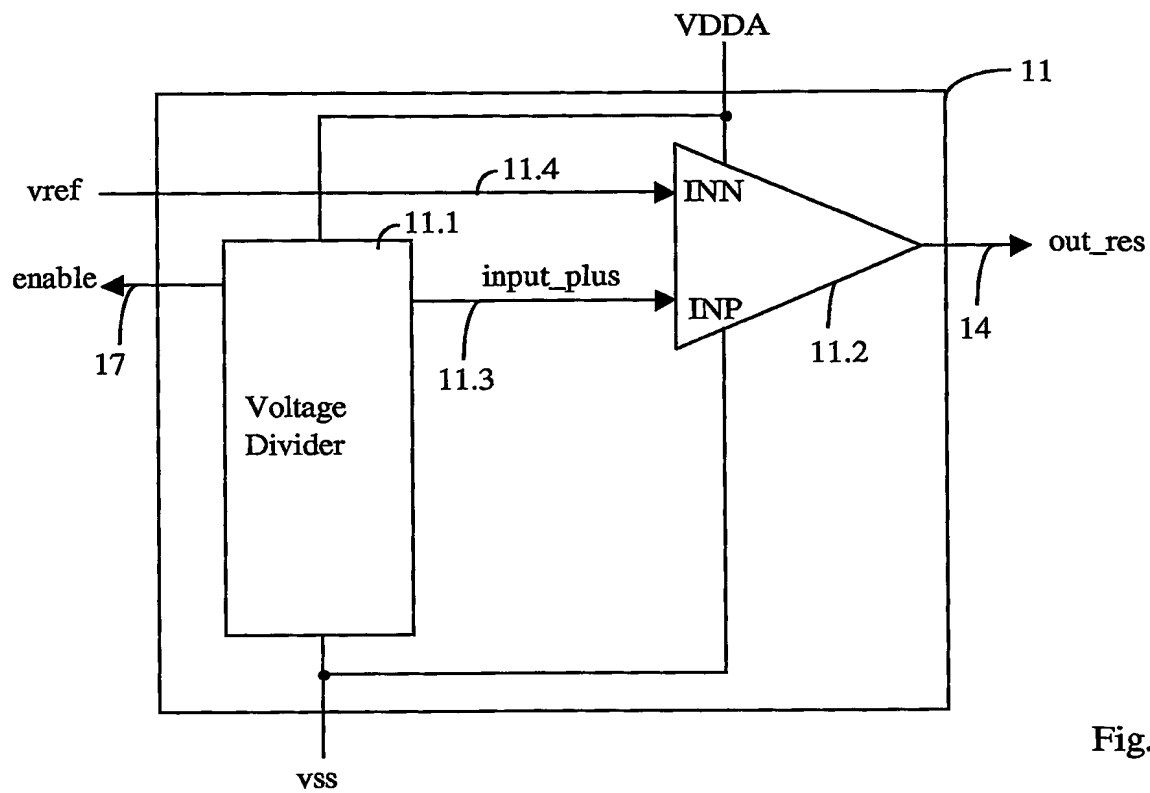


Fig. 1B

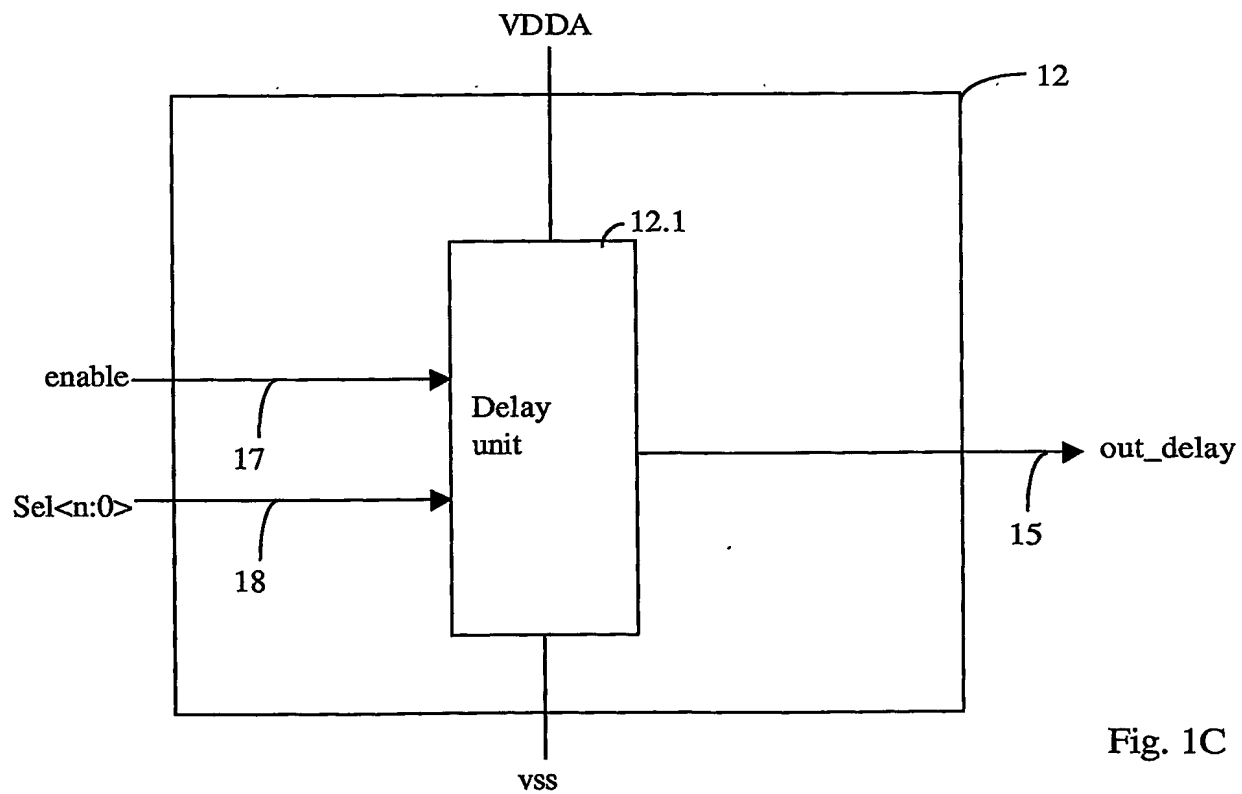


Fig. 1C

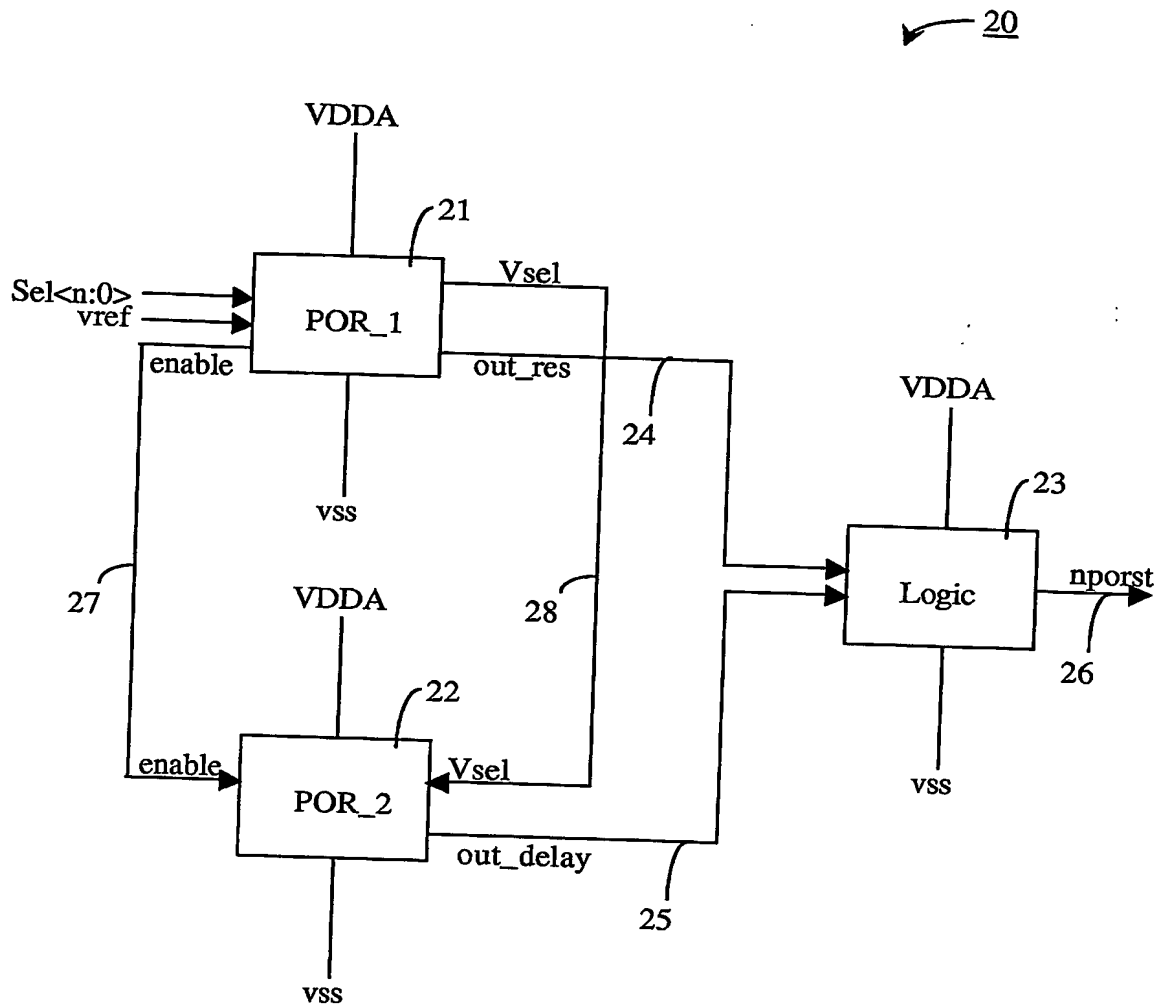


Fig. 2A

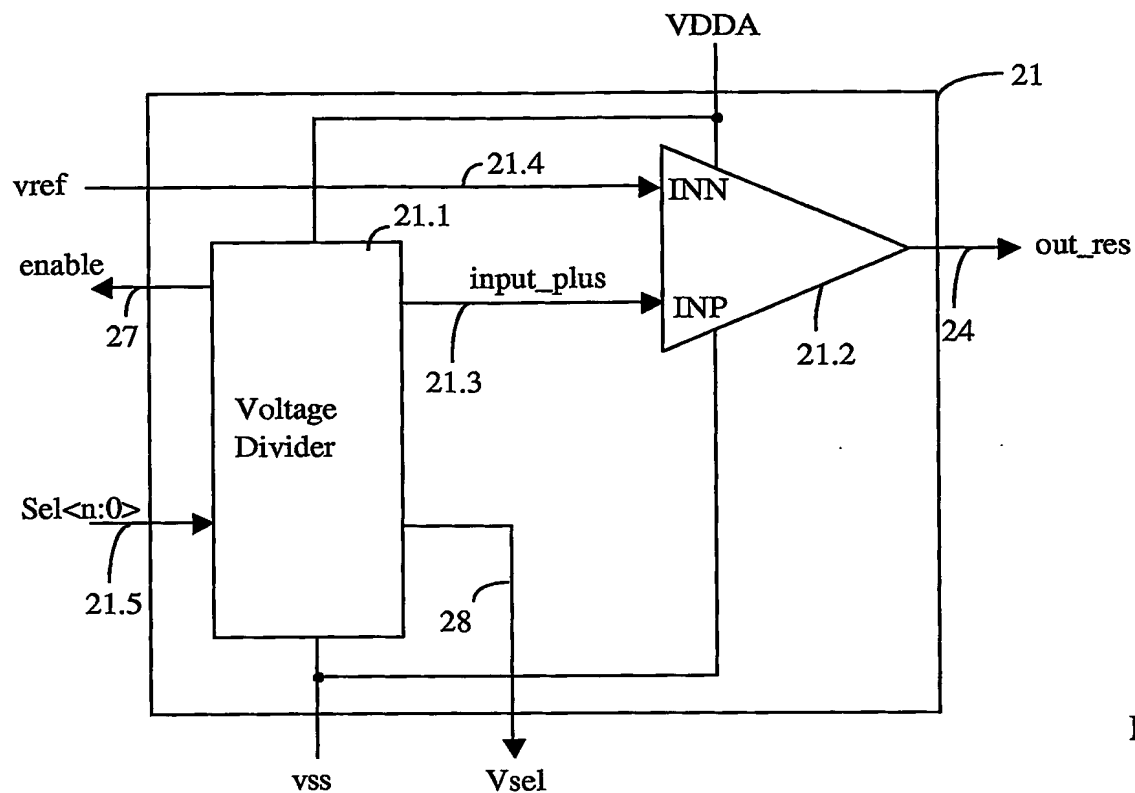


Fig. 2B

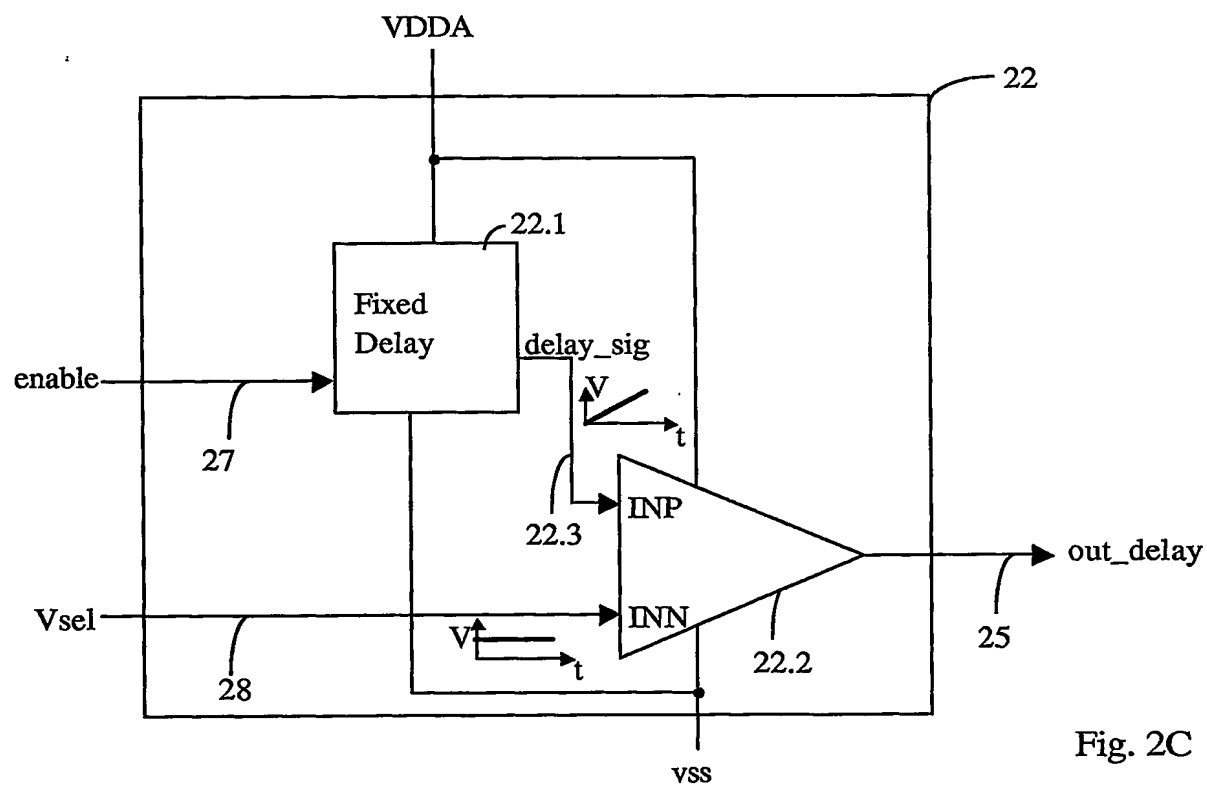


Fig. 2C

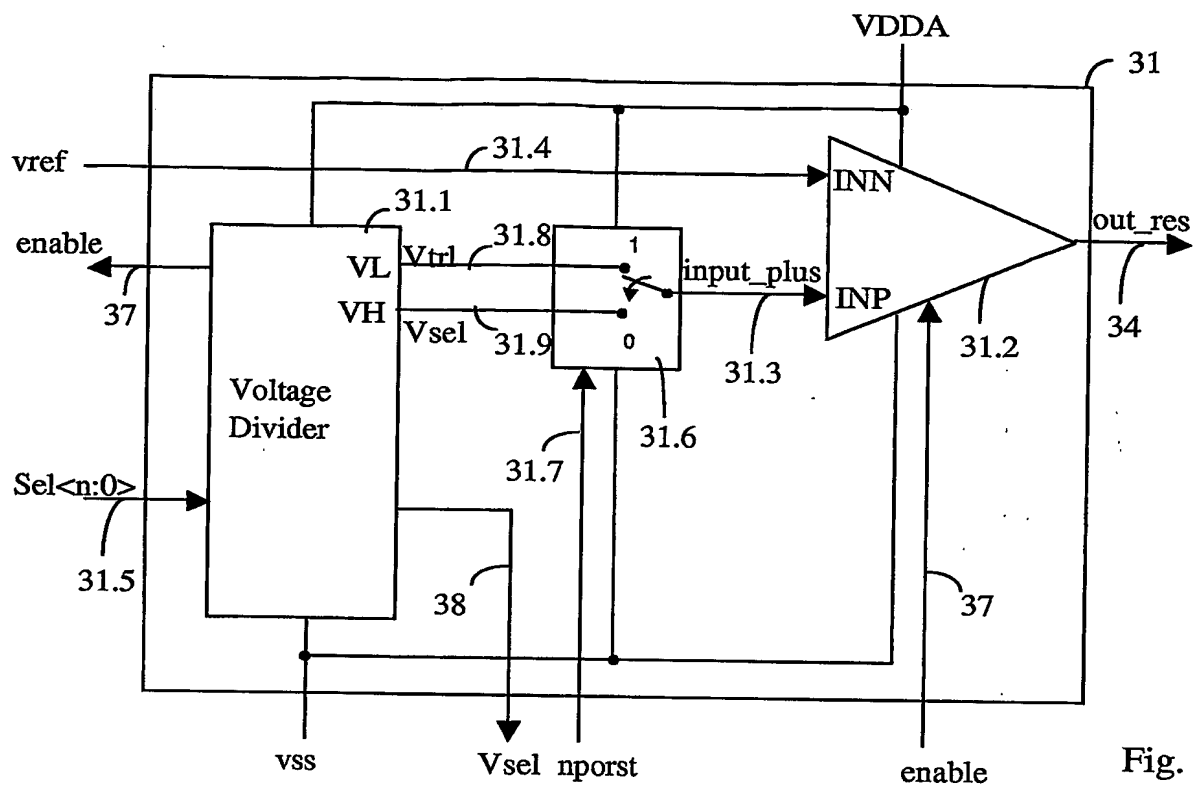


Fig. 3

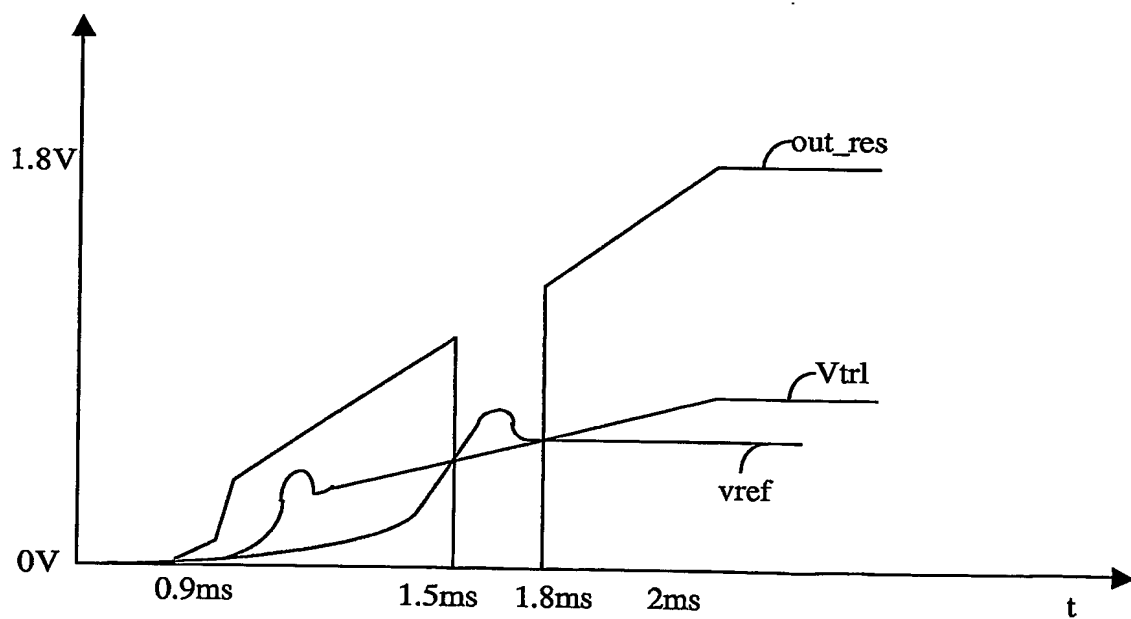


Fig. 4

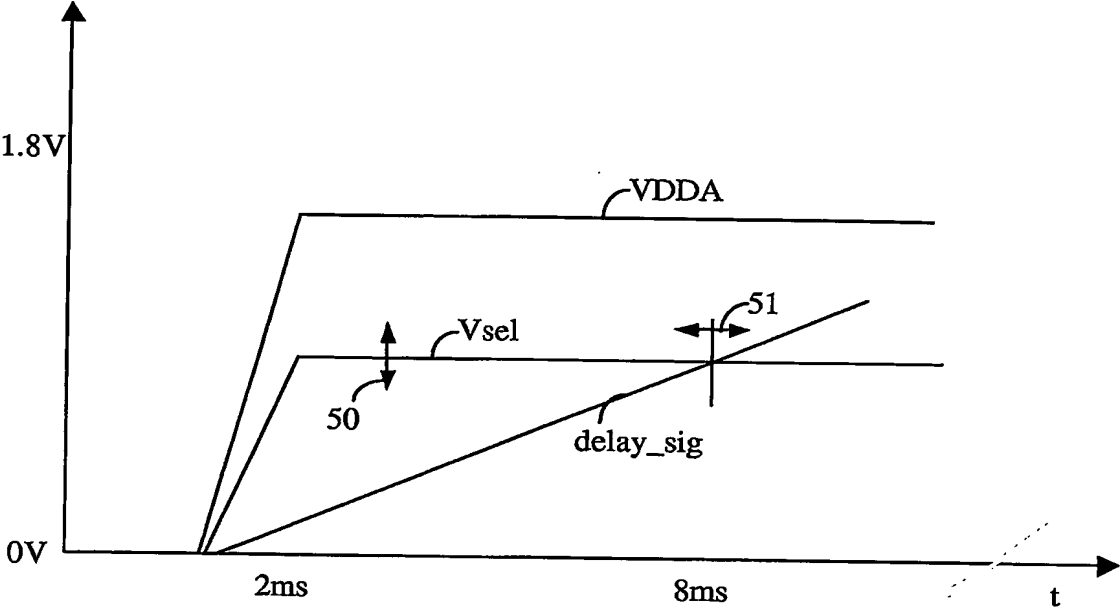


Fig. 5